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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,828	05/27/2005	Makoto Kitabatake	071971-0251	6640
20277	7590	09/25/2006	EXAMINER	
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, N.W. WASHINGTON, DC 20005-3096			KALAM, ABUL	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/536,828	KITABATAKE ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 May 2005 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>5/27/05</u> .   | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the fifth paragraph of 35 U.S.C. 112:

A claim in multiple dependent form shall contain a reference, in the alternative only, to more than one claim previously set forth and then specify a further limitation of the subject matter claimed. A multiple dependent claim shall not serve as a basis for any other multiple dependent claim. A multiple dependent claim shall be construed to incorporate by reference all the limitations of the particular claim in relation to which it is being considered.

2. **Claims 7-11** are rejected under 35 U.S.C. 112, fifth paragraph, as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. Accordingly, claims 7-11 have not been further treated on the merits.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Huang (US 2001/0045644)** in view of **Litwin (US 6,507,047)**.

With respect to **claim 1**, **Huang** teaches a semiconductor apparatus (**FIG. 2**) comprising:

- a semiconductor chip (**230**);
- a base material (**220**) made of an electrically conductive material and connected (**through bonding wires 238**) to a part of a face (**232**) of said semiconductor chip;
- a heat conducting member (**210, 240**) in contact with a part of the face of said semiconductor chip (**230**); and
- an encapsulating material (**242**) for encapsulating said semiconductor chip (**230**) and said heat conducting member (**210, 240**),

wherein a part of said base material (**224**) is extruded outside said encapsulating material (**242**) and works as an external connection terminal (**FIG. 2; pg. 2: [0022]-[0024]**).

Thus, **Huang** teaches all the limitations of the claim, as set forth above, with the exception of explicitly disclosing: wherein the semiconductor chip includes a power semiconductor device constructed by using wide band gap semiconductor.

However, **Litwin** discloses semiconductor chips containing power transistors constructed by using wide band gap semiconductor material (**SiC**) (**col. 1: Ins. 35-67**). **Litwin** discloses that transistors based on silicon carbide, which a well known wide bandgap semiconductor, are another alternative to transistors based on Si or GaAs for power applications at high frequencies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor chip of **Huang** to include wide band

gap semiconductor devices, as taught by **Litwin**, because semiconductor devices based on silicon carbide (SiC) are capable of handling high power densities and can operate at high temperatures, thus improving the speed, reliability and performance of semiconductor chips (**col. 2: Ins. 1-10**).

With respect to **claim 2**, **Huang and Litwin** teach the semiconductor apparatus of claim 1, as set forth above. Regarding the limitation, "wherein said power semiconductor device has a region where a current passes at a current density of 50 A/cm<sup>2</sup> or more," such a claimed range for the current density would have been obvious because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955).

4. **Claims 3 and 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Huang (US 2001/0045644)** and **Litwin (US 6,507,047)**, as applied to claims 1 or 2, and further in view of **Mamitsu et al. (US 6,703,707)**.

With respect to **claim 3**, **Huang and Litwin** teach the semiconductor apparatus of claim 1 or 2, as set forth above. Furthermore, **Huang** discloses wherein said heat conducting member (**210**) is exposed from said encapsulating film (**242**) (**FIG. 2**).

Thus, **Huang and Litwin** teach all the limitations of the claim with the exception of disclosing wherein said encapsulating material is made of resin or glass.

However, **Mamitsu** discloses a semiconductor apparatus wherein the semiconductor chip (**301**) and the heat conducting member (**303, 306**) are encapsulated

with an epoxy based mold resin (**col. 24, Ins. 46-59**). **Mamitsu** teaches that resin is a well known sealing material.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of **Huang and Litwin**, to encapsulate the device using resin, as taught by **Mamitsu**, for the well known purpose of improving durability and reliability of the device.

With respect to **claim 4**, **Huang, Litwin and Mamitsu** teach the semiconductor apparatus of claim 3, as set forth above. Furthermore, **Huang** teaches the apparatus further comprising a radiation fin (**260**) that is in contact with said heat conducting member (**210**) and is extruded outside said encapsulating material (**242**) (**FIG. 5**).

5. **Claims 1, 2 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Teshima (US 2002/0158333)** in view of **Litwin (US 6,507,047)**.

With respect to **claim 1**, **Teshima** teaches a semiconductor apparatus (**FIGS. 1 and 2A-2E**) comprising:

a semiconductor chip (**12**) with including a power semiconductor device (**pg. 2: [0020]**);

a base material (**25a, 25b; FIG. 2C**) made of an electrically conductive material and connected (**through wires 26**) to a part of a face of said semiconductor chip (**12**);

a heat conducting member (**15**) in contact with a part of the face of said semiconductor chip (**12**); and

an encapsulating material **(19)** for encapsulating said semiconductor chip **(12)** and said heat conducting member **(15)**,

wherein a part of said base material **(25a, 25b)** is extruded outside said encapsulating material **(242)** and works as an external connection terminal **(FIGS. 1 and 2A-2E; pgs. 1-2: [0019]-[0029])**.

Thus, **Teshima** teaches all the limitations of the claim, as set forth above, with the exception of explicitly disclosing: wherein the power semiconductor device is constructed by using wide band gap semiconductor.

However, **Litwin** discloses semiconductor chips containing power transistors constructed by using wide band gap semiconductor material **(SiC) (col. 1: Ins. 35-67)**. **Litwin** discloses that transistors based on silicon carbide, which a well known wide bandgap semiconductor, are another alternative to transistors based on Si or GaAs for power applications at high frequencies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor chip of **Teshima** to include wide band gap semiconductor devices, as taught by **Litwin**, because semiconductor devices based on silicon carbide (SiC) are capable of handling high power densities and can operate at high temperatures, thus improving the speed, reliability and performance of semiconductor chips **(col. 2: Ins. 1-10)**.

With respect to **claim 2**, **Teshima and Litwin** teach the semiconductor apparatus of claim 1, as set forth above. Regarding the limitation, "wherein said power semiconductor device has a region where a current passes at a current density of 50

A/cm<sup>2</sup> or more," such a claimed range for the current density would have been obvious because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955).

With respect to **claim 5**, **Teshima and Litwin** teach the semiconductor apparatus of claim 1 or 2, as set forth above. Furthermore, **Teshima** teaches the apparatus further comprising a film **(20)** for covering said encapsulating material **(19)** (**FIG. 1; pg. 2: [0025]**).

6. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Teshima (US 2002/0158333)** and **Litwin (US 6,507,047)**, as applied to claim 5 above, and further in view of **Patil et al. (US 5,227,663)**.

With respect to **claim 6**, **Teshima and Litwin** teach the all the limitations of the claim, as set forth above in claim 5, with the exception of disclosing: the apparatus further comprising a radiation fin opposing said heat conducting member with said film sandwiched therebetween.

However, **Patil** teaches a semiconductor chip package wherein a radiation fin **(96)** opposes a heat conducting member **(82)** with a film **(adhesive)** sandwiched therebetween (**FIG. 3; col. 8: Ins. 29-67; col. 9: Ins. 1-23**).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a radiation fin to the apparatus of **Teshima and Litwin**, as taught by **Patil**, for the disclosed intended purpose of providing additional heat

dissipation, thereby improving the reliability and performance of the device (**col. 9: Ins. 3-16**).

7. **Claims 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin (US 6,184,580)** in view of **Litwin (US 6,507,047)**.

With respect to **claim 12**, **Lin** teaches a semiconductor apparatus (**FIG. 4**) comprising:

a semiconductor chip (**20**);

a base material (**32, 35**) made of an electrically conductive material and connected (**through wires 25 and 27**) to a part of a face of said semiconductor chip (**20**);

a heat conducting member (**42**) in contact with a part of the face of said semiconductor chip (**20**);

a vessel (**formed by carrier 45 and board 60**) in contact with said heat conducting member (**42**) and encapsulating said semiconductor chip (**20**), said base material (**32, 35**) and said heat conducting member (**42**); and

an external connection terminal (**34**) electrically connected to said base material (**32, 35**) and extruded from said vessel (**FIG. 4; col. 3: Ins. 49-67; col. 4: Ins. 1-67; col. 5: Ins. 1-67; col. 6: Ins. 1-19**).

Thus, **Lin** teaches all the limitations of the claim with the exception of disclosing: wherein the semiconductor chip includes a power semiconductor device constructed by using wide band gap semiconductor.

However, **Litwin** discloses semiconductor chips containing power transistors constructed by using wide band gap semiconductor material (**SiC**) (**col. 1: Ins. 35-67**). **Litwin** discloses that transistors based on silicon carbide, which a well known wide bandgap semiconductor, are another alternative to transistors based on Si or GaAs for power applications at high frequencies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor chip of **Lin** to include wide band gap semiconductor devices, as taught by **Litwin**, because semiconductor devices based on silicon carbide (SiC) are capable of handling high power densities and can operate at high temperatures, thus improving the speed, reliability and performance of semiconductor chips (**col. 2: Ins. 1-10**).

With respect to **claim 13**, **Lin** and **Litwin** teach the semiconductor apparatus of claim 12, as set forth above. Furthermore, **Lin** teaches wherein a region around said semiconductor chip (**20**), said base material (**32, 35**) and said heat conducting member (**42**) within said vessel (**formed by carrier 45 and board 60**) is filled with a resin (**col. 4: Ins. 56-62**).

8. **Claims 12 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kurokawa (5,455,457)** in view of **Litwin (US 6,507,047)**.

With respect to **claim 12**, **Kurokawa** teaches a semiconductor apparatus (**FIG. 2**) comprising:

- a semiconductor chip (**1**);
- a base material (**steps of substrate 2**) made of an electrically conductive material and connected (**through wires 4**) to a part of a face of said semiconductor chip (**1**);
- a heat conducting member (**9**) in contact with a part of the face of said semiconductor chip (**1**);
- a vessel (**formed by package substrate 2 and metal cap 6**) in contact with said heat conducting member (**9**) and encapsulating said semiconductor chip (**1**), said base material and said heat conducting member (**9**); and
- an external connection terminal (**3**) electrically connected to said base material and extruded from said vessel (**FIG. 2; col. 5: Ins. 1-35**).

Thus, **Kurokawa** teaches all the limitations of the claim with the exception of disclosing: wherein the semiconductor chip includes a power semiconductor device constructed by using wide band gap semiconductor.

However, **Litwin** discloses semiconductor chips containing power transistors constructed by using wide band gap semiconductor material (**SiC**) (**col. 1: Ins. 35-67**). **Litwin** discloses that transistors based on silicon carbide, which a well known wide bandgap semiconductor, are another alternative to transistors based on Si or GaAs for power applications at high frequencies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor chip of **Kurokawa** to include wide band gap semiconductor devices, as taught by **Litwin**, because semiconductor devices based on silicon carbide (SiC) are capable of handling high power densities and can operate at high temperatures, thus improving the speed, reliability and performance of semiconductor chips (**col. 2: Ins. 1-10**).

With respect to **claim 14**, **Kurokawa** and **Litwin** teach the semiconductor apparatus of claim 12, as set forth above. Furthermore, **Kurokawa** teaches the apparatus further comprising a radiation fin (7) opposing said heat conducting member (9) with a part of said vessel (6) sandwiched therebetween (**FIG. 2; col. 5, Ins. 18-35**).

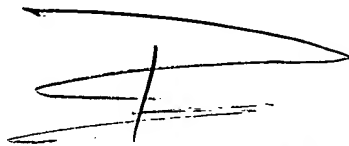
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abul Kalam



**THAO X. LE**  
**PRIMARY PATENT EXAMINER**